REMARKS

This paper is responsive to any paper(s) indicated above, and is responsive in any other manner indicated below.

REQUEST FOR CLARIFICATION – 119 PRIORITY CLAIM

Items 12 a), b), c) of the Office Action Summary page of the Office Action contains checkboxes for the Examiner to designate whether "All", "Some" or "None Of" the certified copies of the priority documents have been received, and no such checkbox has been checked. It is respectfully submitted that "All" of Applicant's certified copies had been previously filed/received within an ancestor application, and according, Applicant respectfully requests that item 12 a) be check within any further communication from the USPTO.

PENDING CLAIMS

Claims 29-61 were pending, under consideration and subjected to examination in the Office Action. Appropriate claims have been amended and/or added (without prejudice or disclaimer) in order to adjust a clarity of Applicant's claimed invention. That is, such changes are unrelated to any prior art or scope adjustment and are simply clarified claims in which Applicant is present interested. At entry of this paper, Claims 29-67 will be pending for further consideration and examination in the application.

REJECTION UNDER 35 USC '102

The 35 USC '102 rejection of claims 29-61 as being anticipated by Yamagami et al. (U.S. Patent 5,644,539) is respectfully traversed. All descriptions of Applicant's disclosed and claimed invention, and all descriptions and rebuttal arguments regarding the applied prior art, as previously submitted by Applicant in any form, are repeated and incorporated hereat by reference. Further, all Office Action statements regarding the prior art rejections are respectfully traversed. As additional arguments, Applicant respectfully submits the following.

In order to properly support a '102 anticipatory-type rejection, any applied art reference must disclose each and every limitation of any rejected claim. The applied art does not adequately support a '102 anticipatory-type rejection because, at minimum, such applied art does not disclose (or suggest) the following discussed limitations of Applicant's claims.

Applicant's disclosed and claimed arrangements are directed toward achieving storage device arrangements where an error correcting operation can be applied (to insure integrity of data), while at the same time, any time penalty associated with the error correcting operation can be avoided (i.e., hidden) from the host system. In order to accomplish the same, Applicant's disclosed and claimed "controller carries out **concurrent** (or **parallel**; or **overlapping**) operations of: data transferring of data after data processing to said host system via said system interface unit, and data transferring of subsequent data for data processing from said non-volatile semiconductor memory to said controller."

That is, while Applicant's arrangements output one set (e.g., a sector) of data, it is concurrently loading a next set (e.g., sector) of data for error correction. Loading/analyzing a next set of data (for error correction) during the same time as outputting a current set of data, allows no additional time (i.e., penalty) to be incurred for the error correcting operation.

Regarding rebuttal of Yamagami et al. reference, in short, such reference does not disclose or suggest any type of arrangement wherein a "controller carries out **concurrent** (or **parallel**; or **overlapping**) operations of: data transferring of data after data processing to said host system via said system interface unit, and data transferring of subsequent data for data processing from said non-volatile semiconductor memory to said controller." Instead, a main gist of Yamagami et al. is to allow substitute blocks of memory to be utilized instead of defective blocks of memory (e.g., within a flash memory), such that a memory device can be repaired and/or have a useful life thereof extended. The Yamagami et al. FIGS, Columns, Lines cited within the Office Action only pertain to generalized teachings regarding a layout of the Yamagami et al. configuration.

In addition to the foregoing, the following additional remarks from Applicant's foreign representative are also submitted in support of traversal of the rejection and patentability of Applicant's claims.

Regarding arguments to the rejection under 35 U.S.C. §102(e), as can be seen in the present claims 29, 40 and 51, a subject matter of the present invention is "wherein, in response to a read command received by the system interface unit, the controller carries out concurrent operations, parallel operations

or overlap operations of data transferring of data after data processing to the host system via the system interface unit and of data transferring of subsequent data for data processing from the non-volatile semiconductor memory to the controller".

Yamagami et al (United States Patent No. No. 5,644,539) discloses a semiconductor disk storage device which is connected to the host bus 3 of a host system 2 and comprises a microcomputer 4 (functioning as logical area conversion means, instruction acceptance means and instruction conversion means), a memory controller 5, a buffer memory 6, an error memory 7 and a data memory 8 (Fig. 1, col. 4, lines 29-36). For argument purposes, the semiconductor disk storage device of Yamagami et al corresponds to the storage device of the present invention, the microcomputer 4 and the memory controller 5 of Yamagami et al correspond to the controller of the present invention, and the data memory 8 of Yamagami et al corresponds to the non-volatile semiconductor memory of the present invention.

According to the detailed action, the Examiner points out that Yamagami et al discloses the above subject matter of Applicant's present invention in Fig. 1, col. 4, lines 25-56, col. 12, lines 38-45. However, Yamagami et al only discloses in col. 4, lines 49-56, that the "microcomputer 4 receives an instruction from the host bus 3, and controls the memory controller 5 in accordance with the instruction. The memory controller 5 controls the read and write operations of the buffer memory 6, error memory 7 and data memory 8 by the use of addresses 9, data 10 and control signals 11. In addition, since the error memory

7 and the data memory 8 require erase operations, the memory controller 5 controls the erase operations." More particularly, such cited passage does not disclose that the microcomputer 4 or the memory controller 5, in response to a read instruction from the host system 2, carries out concurrent operations, parallel operations or overlap operations of data transferring of data after data processing to the host system 2 and of data transferring of subsequent data for data processing from data memory 8 to the microcomputer 4 or the memory controller 5. Namely, Yamagami et al does not disclose the above subject matter of the present invention.

As a result of all of the foregoing, it is respectfully submitted that the applied art would not support a '102 anticipatory-type rejection of Applicant's claims. Accordingly, reconsideration and withdrawal of such '102 rejection, and express written allowance of all of the '102 rejected claims, are respectfully requested. Further, at this point, it is respectfully submitted as a reminder that, if new art is now cited against any of Applicant's prior claims (only very minorly amended), then it would not be proper to make a next action final.

EXTENSIVE PROSECUTION NOTED

Applicant and the undersigned respectfully note the extensive prosecution which has been conducted to date with the present application, and thus Applicant and the undersigned would gratefully appreciate any considerations or guidance from the Examiner to help move the present application quickly to allowance.

EXAMINER INVITED TO TELEPHONE

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703/312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

RESERVATION OF RIGHTS

It is respectfully submitted that any and all claim amendments and/or cancellations submitted within this paper and throughout prosecution of the present application are without prejudice or disclaimer. That is, any above statements, or any present amendment or cancellation of claims (all made without prejudice or disclaimer), should not be taken as an indication or admission that any objection/rejection was valid, or as a disclaimer of any scope or subject matter. Applicant respectfully reserves all rights to file subsequent related application(s) (including reissue applications) directed to any/all previously claimed limitations/features which have been subsequently amended or cancelled, or to any/all limitations/features not yet claimed, i.e., Applicant continues (indefinitely) to maintain no intention or desire to dedicate or surrender any limitations/features of subject matter of the present application to the public.